PVS: Pacemaker Verification System
A Real-Time Heart Model on a Chip

Abstract

There are currently about 3 million individuals in the world who depend on pacemakers, which are surgically implanted devices that maintain proper heart rhythm. Pacemakers, complex as they are, are programmed with tens of thousands of lines of code, and are therefore inevitably prone to bugs. It may not come as a surprise then that between 1990 and 2000, over 200,000 pacemakers were recalled due to software issues.

The purpose of the Pacemaker Verification System, then, is to test pacemakers with the realism of clinical trials but without their risks, with the goal of finding software errors before patient implantation. Our system addresses this problem with a virtual heart that can be reconfigured to exhibit different arrhythmias. The virtual heart was built by using finite state machines to model the heart's signal propagation properties for these different arrhythmias. Using code generation tools, these models were then directly translated to an FPGA hardware implementation, ensuring that the behavior of the models was retained.

This virtual heart is able to interface with pacemakers and react to them in a manner that mimics a real heart. It can both output heart beats to the pacemaker and react to paces from the pacemaker. A top-level user interface allows manufacturers, regulators, and cardiologists to view the results of this closed-loop, dynamic system. Such a system allows for interactions that no static heart model can provide, thus offering more robust testing methods and thereby saving lives.

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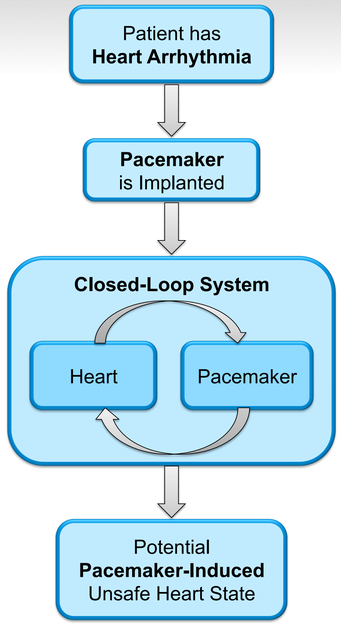
Problem



Irregular heartbeat potentially has grievous consequences

Requires invasive surgery

Static code analysis and unit testing cannot capture *closed-loop* interactions between the heart and pacemaker

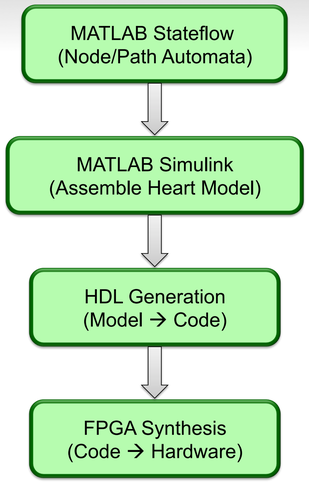
Need to capture these high-risk and possibly fatal errors **before** patient implantation

Idea

- **Build a virtual heart to implement a closed-loop testing framework**
  - Models heart electrophysiology
  - FPGA-based hardware platform
  - Electrical interface with pacemaker
  - Allows for the monitoring of dynamic heart-pacemaker interactions
- **Employ model-based development**
  - Seamless transition between simulation and real-world testing
  - Easily extensible
- **Provide for virtual heart reconfiguration at runtime**
  - Emulates a variety of arrhythmias
  - Provides realistic testing scenarios for pacemakers

Software Toolchain

For Generating Virtual Heart Model

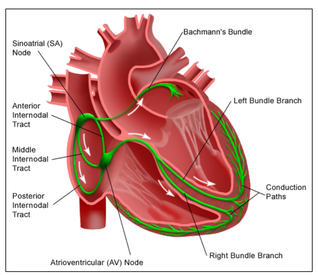


Entire process is automated in accordance with the principles of **Model-Based Development**

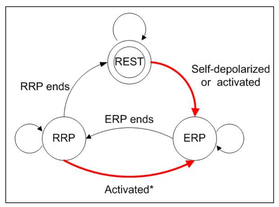
How To Model a Heart

- Heart beats in response to a self-generated periodic electrical pulse
- The subsequent signal propagation is analogous to an electrical circuit with nodes and connections between nodes ("paths")
- Prior research in the mLAB modeled the timing parameters of these nodes and paths using finite state automata

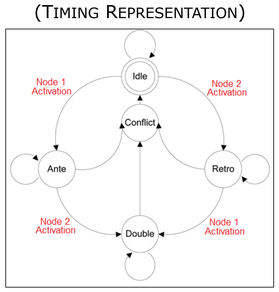
Electrical System of the Heart



Node Automata (Timing Representation)

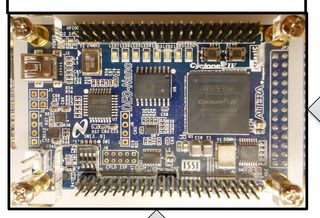


Path Automata (Timing Representation)

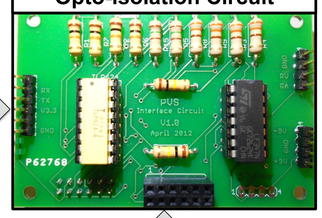


Implementation

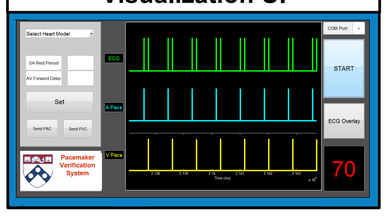
Heart on a Chip



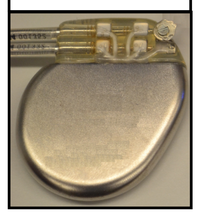
Custom Attenuation and Opto-isolation Circuit



Configuration and Visualization UI



Pacemaker



Results

- Modeled and implemented a virtual heart that can be configured with various arrhythmias
- Established a bidirectional interface between virtual heart and pacemaker
- Realized closed-loop feedback system
  - Normal heart rate does not induce pacing of virtual heart
  - Slow heart rate (Bradycardia) results in corrective measures from the pacemaker
- **Successfully captures pacemaker-induced unsafe heart state (Endless Loop Tachycardia)**
  - Sequence of Events
    1. Heart has normal rhythm
    2. Single extra beat occurs that is not normally harmful for the heart
    3. False positive feedback loop occurs in pacemaker, resulting in a dangerously high heart rate